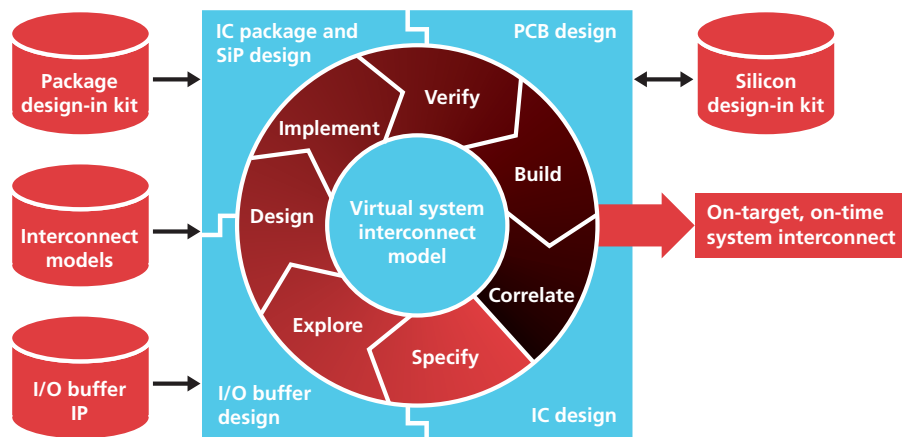


ALLEGRO PCB SI L, XL ALLEGRO PCB PI OPTION XL

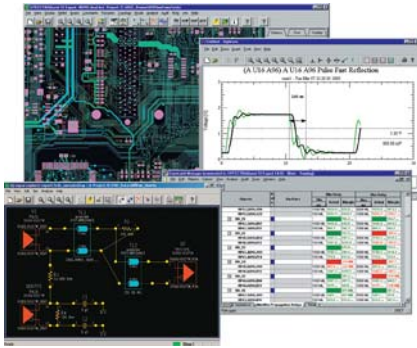
Cadence® Allegro® PCB SI offers an integrated high-speed design and analysis environment to streamline the creation of high-speed digital printed circuit board (PCB) systems. Its advanced capabilities make it easy for electrical engineers to explore, optimize, and resolve electrical performance-related issues at all stages of the design cycle. A constraint-driven design flow increases the likelihood of first-time success and reduces overall product cost.



The Allegro system interconnect design platform

THE ALLEGRO SYSTEM INTERCONNECT DESIGN PLATFORM

The Cadence Allegro system interconnect design platform enables collaborative design of high-performance interconnect across IC, package, and PCB domains. The platform’s unique co-design methodology optimizes system interconnect—between I/O buffers and across ICs, packages, and PCBs—to eliminate hardware re-spins, decrease costs, and reduce design cycles. The constraint-driven Allegro flow offers advanced capabilities for design capture, signal integrity, and physical implementation. With associated silicon design-in IP portfolios, IC companies shorten new device adoption time and systems companies accelerate PCB design cycles for rapid time to profit. Supported by the Cadence Encounter® and Virtuoso® platforms, the Allegro co-design methodology ensures effective design chain collaboration.



Allegro PCB SI allows engineers to explore and develop optimum constraints with a constraint-driven design flow

ALLEGRO PCB SI

Allegro PCB SI provides advanced analysis at the board, multi-board, and/or system level, and across multiple design configurations. It supports the entire high-speed design flow, which includes pre-layout exploration of design parameters such as differential impedance, development of physical parameters, and imprinting of constraints within the PCB database. The result is a true, constraint-driven design flow. Allegro PCB SI integrates tightly with Allegro PCB Editor, Allegro PCB Router, and Allegro Design Entry HDL enabling end-to-end, constraint-driven, high-speed PCB system design.

Allegro PCB SI addresses the challenges created as a result of increasing design density, complexity, and faster edge rates by enabling designers to address high-speed issues throughout the design process. This approach allows design teams to eliminate time-consuming simulate-fix-simulate iterations at the back-end of a design. It also enables designers to maximize electrical performance while minimizing cost of the overall product by exploring topologies and models with manufacturing tolerances. Allegro PCB SI allows users to weigh the tradeoffs involved in routing choices (rules) that affect cost relative

to electrical performance and reliability. Once developed, these optimal constraints then drive the physical layout and routing of the PCB. The integrated design and analysis environment eliminates the need to translate design databases to run simulations. Designers can also address shrinking timing margins by considering the effects of package design on the overall performance of the signal from die-to-die. Importantly, the integrated flow allows designers to easily perform post-layout extraction and verification of complex high-speed PCB systems.

BENEFITS

- Cuts the time required to design high-speed interconnects and increases the likelihood of first-pass success
- Shortens the time required to develop optimum constraints and enables a constraint-driven PCB design flow
- Shortens the time required to design-in advanced devices through the use of Cadence design-in IP portfolios
- Improves product performance through solution space exploration
- Reduces unit costs of end products by using the Allegro PCB PI Option XL to design the PCB power delivery system network

FEATURES

INTEGRATED HIGH-SPEED DESIGN AND ANALYSIS

Allegro PCB SI reads and writes to the Allegro PCB Editor database to avoid possible translation issues and allows for constraints and models to be embedded in the board design file. The integrated design and analysis system is aware of multi-net electrical constructs from front to back. For example, differential pairs and extended nets (nets with a series termination) are recognized, extracted, and simulated as one electrical net.

SOLUTION SPACE EXPLORATION

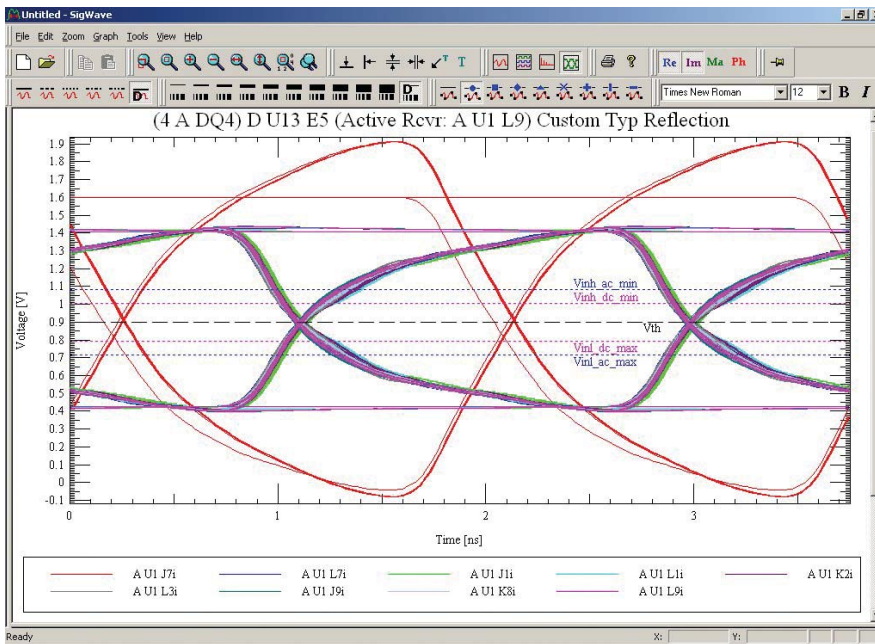
Allegro PCB SI provides the best environment for users who need to develop optimal constraints. SigXplorer, a graphical editor that allows designers to develop constraints through solution space exploration, is the industry leader in pre-route analysis. Solve issues early in the design process by using swept parameter analysis, user-defined stimulus, and custom measurements.

SPICE-BASED SIMULATOR

The Allegro PCB SI simulation subsystem includes a SPICE-based simulator as well as a powerful macro-modeling capability that combines the advantages of traditional SPICE-based structural modeling with the speed of behavioral modeling. An embedded field solver models skin effects, proximity/crowding effects, return path resistance, and frequency-dependent dielectric constant. A robust modeling language provides extensibility beyond IBIS for I/O buffers and lossy coupled, frequency-dependent transmission line models that accurately predict the distributed behavior of PCB traces.

BUS ANALYSIS FOR SOURCE SYNCHRONOUS SIGNALS

Allegro PCB SI provides a quick and easy way to analyze all the signals associated with a source synchronous bus. It shortens the time to simulate various configurations (read/write, active, idle) associated with the functioning of source synchronous buses with or without on-die termination (ODT). It allows signals to be associated and to save such associations with the design database.



Allegro PCB SI allows engineers to explore and develop optimum constraints with a constraint-driven design flow

DIE-TO-DIE INTERCONNECT ANALYSIS USING PACKAGE DATABASES

Allegro PCB SI supports multi-board configurations for both analysis and constraints, and provides a simple setup process—from motherboard or daughter card connection to a die-to-die configuration. It also supports topology exploration, floorplanning, and post-route verification.

CONSTRAINT-DRIVEN PROCESS

Allegro Constraint Manager functions within Allegro PCB SI, Allegro Design Entry HDL, and with Allegro PCB Design XL, allowing designers to use constraints developed through solution space exploration to create a constraint-driven physical layout process.

MODEL INTEGRITY

The Model Integrity module allows designers to create, manipulate, and validate models quickly in an easy-to-use editing environment. Device model formats supported include:

- IBIS 4.1 External Model support for Verilog®-A, Cadence Spectre®, HSPICE, Cadence eSpice models
- Mentor/Quad XTK
- Cadence Device Modeling Language (DML)

A Spectre-to-DML conversion module assists in creating DML models from Spectre simulation runs. With the output of the Spectre simulation run, buffer options file, users can quickly create DML models. Model integrity identifies V-I and V-T tables for typical, maximum, and minimum corner cases

from the Spectre run file. A proven, intelligent best-curve-fitting algorithm provides an accurate DML model. An HSPICE-to-IBIS conversion module allows users to create IBIS models from HSPICE simulation runs.

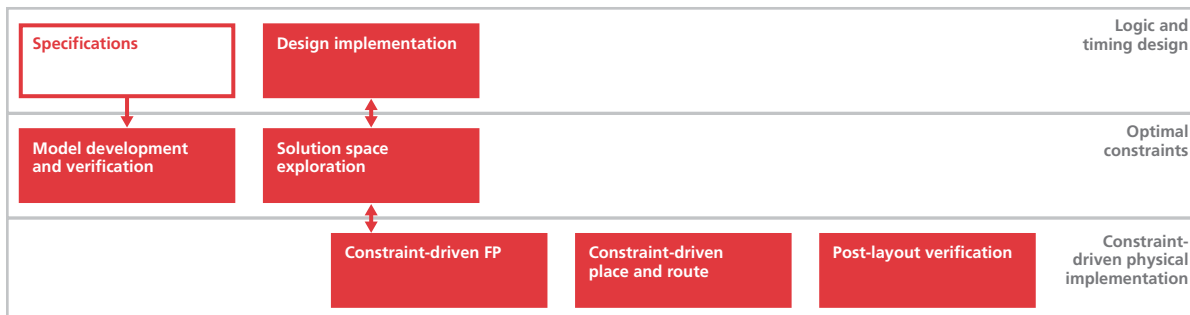
I/O BUFFER MODELS

Supported I/O buffer model formats include:

- Cadence Allegro PCB SI DML
- Synopsys HSPICE transistor-level models (requires HSPICE simulator and license, which is not included with Allegro PCB SI)
- Spectre transistor-level models (available on Sun Solaris, HP UX, and Linux RHEL 3.0 platforms only). This utilizes an integrated and limited capability version of the Spectre simulator, which is included with Allegro PCB SI XL
- IBIS 4.1 External Model support for HSPICE, Spectre, Verilog-A and Cadence DML
- Mentor/Quad XTK

MENTOR BOARD STATION FLOW

Allegro PCB SI can be used in conjunction with the Mentor Board Station PCB design system to provide high-speed design and analysis within a Mentor-based PCB design environment. Allegro PCB SI is used to perform high-speed analysis and to define the high-speed design rules used to drive the Allegro PCB Router. Once the design has been placed and routed in accordance with the high-speed rules, the results are passed back to the Mentor Board Station environment. This allows Allegro PCB SI and the Allegro PCB Router to be



Allegro PCB SI enables a constraint-driven flow that shortens the design cycle and increases the likelihood of first-pass success

used for high-speed design and analysis, while the existing Board Station-based manufacturing output process is used for committing the design to manufacturing.

DESIGN-IN IP PORTFOLIO

A high-speed design-in IP portfolio shortens design-in time for complex devices with high-speed digital I/O buffers. Cadence pioneered this concept by introducing an IP portfolio for Intel's 64-bit architecture and today stands as the industry leader in offering this kind of complete solution. Design-in IP portfolio contains ready-to-simulate topologies with pre-validated models, layout constraints embedded in a sample PCB file to enable constraint-driven layout flows, tutorials, documentation, scripts, and other utilities. A high-speed design-in IP portfolio includes prepackaged, executable specifications for complex IC devices with high-speed I/Os. Cadence collaborates with IC companies to make it easy for systems companies to design-in complex IC devices with high-speed I/Os.

PCI EXPRESS DESIGN CHAIN

As multi-gigahertz serial interfaces become more common, many systems companies are choosing to use the next-generation PCI bus—PCI Express. The PCI Express design chain provides an environment in which silicon vendors can communicate the design-in requirements for their devices using PCI Express. Systems companies are able to make tradeoffs regarding the performance of member companies' silicon with respect to system requirements.

The PCI Express design chain is web-based infrastructure that enables systems companies that design serial links implementing the PCI Express specification to efficiently qualify member companies as candidates for their systems. For more information about other design-in IP portfolios and the PCI Express design chain, visit www.cdnusers.org.

INTEL IXP2800 NETWORK PROCESSOR DESIGN-IN IP PORTFOLIO

Intel and Cadence engineers worked together to provide a high-speed design-in IP portfolio for Intel's IXP2800 network processor. Available from Intel and included in the hardware design kit for IXP2800, the design-in IP portfolio contains ready-to-simulate system-level topologies for the buses that interact with the network processor (RDRAM, SPI4.2, PCI, and QDR); correlated silicon models; a fully coupled frequency-dependent lossy package; and PCB trace, via, and connector models to fully simulate and evaluate the signal quality and degradation issues inherent in designs with high-speed nets. In addition, the design-in IP portfolio contains a reference board that includes the constraints for the main buses on the processor. This reference board and the constraint sets can be used to drive floorplanning, placement, and routing on the target PCB system that uses the IXP2800 networking processor. The ready-to-simulate topologies come with instructions on how to use these topologies, as well as movies that show how to use the design-in IP portfolio with Allegro PCB SI. For more information, contact your Intel representative and ask for the hardware design kit (HDK) for the IXP2800 network processor.

XILINX VIRTEX II-PRO DESIGN-IN IP PORTFOLIO

Xilinx and Cadence engineers worked together to provide a high-speed design-in IP portfolio in Allegro PCB SI format for multi-gigabit serial Rocket I/O transceivers integrated in Xilinx Virtex II-Pro FPGAs. The Allegro PCB SI design-in IP portfolio helps engineers shorten design cycles and reduce signal integrity problems when implementing multi-gigabit serial transceivers in PCB systems. It contains correlated silicon models, preconfigured topologies ready to simulate, and a fully coupled, frequency-dependent lossy package. It also contains PCB trace, via, and connector models to fully simulate and evaluate the signal quality and degradation issues inherent in designs with multi-gigabit

transceivers. For more information, visit www.xilinx.com or contact your Xilinx or Cadence representative.

POWER DELIVERY SYSTEM DESIGN WITH ALLEGRO PCB PI OPTION XL

Allegro PCB PI Option XL module, an add-on to Allegro PCB SI, is a unique, integrated design and analysis environment that takes the guesswork out of quantifying and controlling noise in power delivery systems. It allows users to focus on the design instead of struggling with data translation issues between the CAD system and the analysis engines. It integrates proven technology from Sun Microsystems into the Cadence design and analysis environment to address the power delivery issues encountered in high-speed design.

Allegro PCB PI Option XL embodies a methodology used to design and optimize frequency-dependent characteristics (supply path impedance) of power distribution systems in high-speed PCB design. It allows users to do quick and easy iterations of "change-simulate-analyze." The Cadence approach is rooted in the fact that a power distribution system's impedance is frequency dependent and must be analyzed and controlled over frequency ranges of interest. The maximum supply current and the tolerated voltage ripple are used to derive the main power delivery system's design parameter—the target impedance. Optimizing the target impedance over the frequency range in which the system is expected to operate yields a power delivery system without hot spots.

FEATURES

SETUP WIZARD

The Setup Wizard gathers all the necessary pieces for design and analysis including board outline; layer stack-up; power plane shapes/power and ground plane pairs; DC nets associated with the power planes; and capacitor libraries.

FREQUENCY DOMAIN ANALYSIS

Allegro PCB PI Option XL combines the right frequency domain analysis engine with the proven, powerful Allegro PCB SI and Allegro PCB Editor design environments. It simulates the problem in the frequency domain to quantify the impedance of the power delivery system across the frequency range of interest. During simulation, it takes into account the entire power delivery system—VRM, bulk capacitors, bypass capacitors, and power planes. It calculates the number and values of decoupling capacitors and guides users in placing them for optimal results. Users can perform single node analysis early in the design cycle to see if the number of capacitors selected can maintain the target impedance over a desired frequency range. And, as capacitors are placed on the board, multi-node simulation, which takes into account the location of the capacitors on the board and the mounted loop inductance, can be easily run.

VRM EDITOR

The VRM Editor comes with an easy-to-use input inductance calculator and a target impedance calculator. Specify the allowed voltage ripple and dynamic current to compute the target impedance, and the target impedance is shown in the simulation

results waveform window. The simulation waveform window displays a target impedance line, which makes it easy to know which regions of the PCB are crossing the target.

VOLTAGE RIPPLES IN TIME DOMAIN

Effectiveness of decoupling capacitor selection and placement can be verified in time domain.

COMPLETE DESIGN AND ANALYSIS ENVIRONMENT

Allegro PCB PI Option XL offers a unique approach to the actual designing of power distribution systems. It takes the integrated approach a step further by making the debugging of a problem as simple as “click and view.” Clicking on a waveform in the waveform display window highlights the corresponding region on the PCB and offers a suggestion on the type and number of capacitors needed to address the problem. Results are displayed in the waveform window. By having a PCB design editor integrated with this analysis environment, engineers can select and place decoupling capacitors in the necessary areas, and then quickly see the problem resolved.

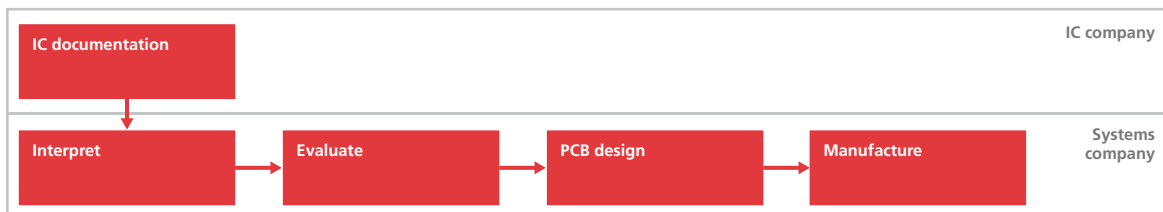
OPERATING SYSTEM SUPPORT

- Red Hat Linux 3.0, 4.0
- Windows 2000 with Service Pack 4, XP Professional
- Sun Solaris 8, 9, 10
- HP-UX 11.11i
- IBM AIX 5.3

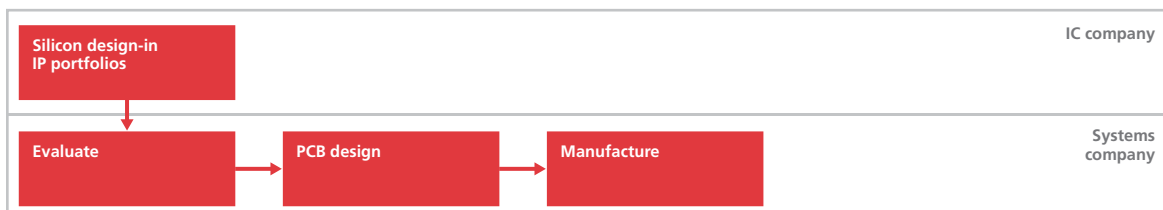
CADENCE SERVICES AND SUPPORT

- Cadence application engineers can answer your technical questions by telephone, email, or Internet—they can also provide technical assistance and custom training
- Cadence certified instructors teach over 70 courses and bring their real-world experience into the classroom
- Over 25 Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet
- SourceLink® online customer support gives you answers to your technical questions—24 hours a day, 7 days a week—including the latest in quarterly software rollups, product change release information, technical documentation, solutions, software updates, and more

DESIGN-IN IP PORTFOLIOS ACCELERATE DESIGN START TIME



Traditional design process for designing-in complex devices with high-speed digital I/Os



High-speed design-in IP portfolios shave weeks or months off design schedules

MAJOR FEATURE SUMMARY FOR ALLEGRO PCB SI PRODUCTS

Major feature summary for Allegro PCB SI XL, Allegro Design Entry HDL SI XL, Allegro PCB SI L, and Allegro PCB PI option XL

| | Allegro PCB SI L | Allegro PCB SI Board L | Allegro Design Entry HDL SI XL | Allegro PCB SI XL | Allegro PCB PI option XL |
|--|------------------|------------------------|--------------------------------|-------------------|--------------------------|
| Allegro Design Entry HDL XL | | | x | | |
| Assign Models in Schematics | | | x | | |
| Create Xnets in Schematics | | | x | | |
| Apply Constraints & Topologies to Schematic for Single-Ended & Differential Nets | | | x | | |
| Single-line Topology Editor (Graphical Canvas) | x | x | x | x | |
| Simulation Setup Advisor | x | x | | x | |
| Model Integrity: Model Development Environment | x | x | x | x | |
| Model Integrity: Syntax Checking for IBIS 3.2 and DML | x | x | x | x | |
| Model Integrity: HSPICE-to-IBIS Conversion | x | x | x | x | |
| IBIS 4.0 Models Support | x | x | x | x | |
| Quad Models Translator | x | x | x | x | |
| Macro-models Support (DML) | x | x | x | x | |
| Simulation Control: Single-line Simulation | x | x | x | x | |
| Waveform Viewer | x | x | x | x | |
| Detailed Simulation Reports (Such as Flight Time, Overshoot, Noise Margin) | x | x | x | x | |
| Coupled (3 Net) Simulation | x | x | | x | |
| Coupled (>3nets) Simulation | | x | | x | |
| Single Net Pre-layout Extraction from Allegro Design Entry HDL | x | x | x | x | |
| Allegro Physical Viewer Plus | x | | | | |
| Differential Pair Exploration and Simulation | x | x | x | x | |
| Differential Pair Pre- and Post-layout Extraction from Allegro PCB Editor | x | x | | x | |
| Differential Pair Pre-layout Extraction from Allegro Design Entry HDL | | x | x | x | |
| Differential Signal Constraint Capture | | x | x | x | |
| Coupled Line Simulations | | x | x | x | |
| Crosstalk Simulation | | x | x | x | |
| Source Synchronous Bus Analysis (SI Board L & SI XL) | | x | x | x | |
| Sweep Simulations | | x | x | x | |
| Current Probes | | x | x | x | |
| Multiterminal Black Boxes in Topologies | | x | x | x | |
| Constraint Development and Capture of Topologies | | x | x | x | |
| Custom Measurement | | x | x | x | |
| Custom Stimulus | | x | x | x | |
| Batch Simulation | | x | | x | |
| EMControl: Rules Development | | x | | x | |
| EMControl: Rules Checking | | x | | x | |
| EMI Differential Simulation | | x | x | x | |
| Allegro Constraint Manager | | x | x | x | |
| Color-coded Real-time Feedback on Violations | | | | x | |
| Apply Constraints and Topologies to Board for Single-ended and Differential Nets | | x | | x | |
| Floorplanner | | x | | x | |
| Constraint-driven Floorplanning and Routing | | x | | x | |
| Allegro PCB Router XL | | | | x | |
| Voltage Ripples in Time Domain | | | | | x |
| Power Integrity: Design and Analysis Environment | | | | | x |
| Power Integrity: Decoupling Capacitor Database Setup Wizard | | | | | x |
| Power Integrity: Impedance Requirements Calculator | | | | | x |
| Power Integrity: Decoupling Capacitor Selection and Placement Environment | | | | | x |
| Power Integrity: VRM Editor | | | | | x |
| Power Integrity: Decoupling Capacitor Library Editor | | | | | x |
| Power Integrity: Cross-probing Between Waveform Allegro PCB SI Floorplanner | | | | | x |
| Power Integrity: Frequency Domain Analysis | | | | | x |

FOR MORE INFORMATION

Contact Cadence sales at 1.800.746.6223
or visit www.cadence.com for
additional information. To locate a
Cadence sales office or Cadence
Channel Partner in your area, visit
www.cadence.com/contact_us.